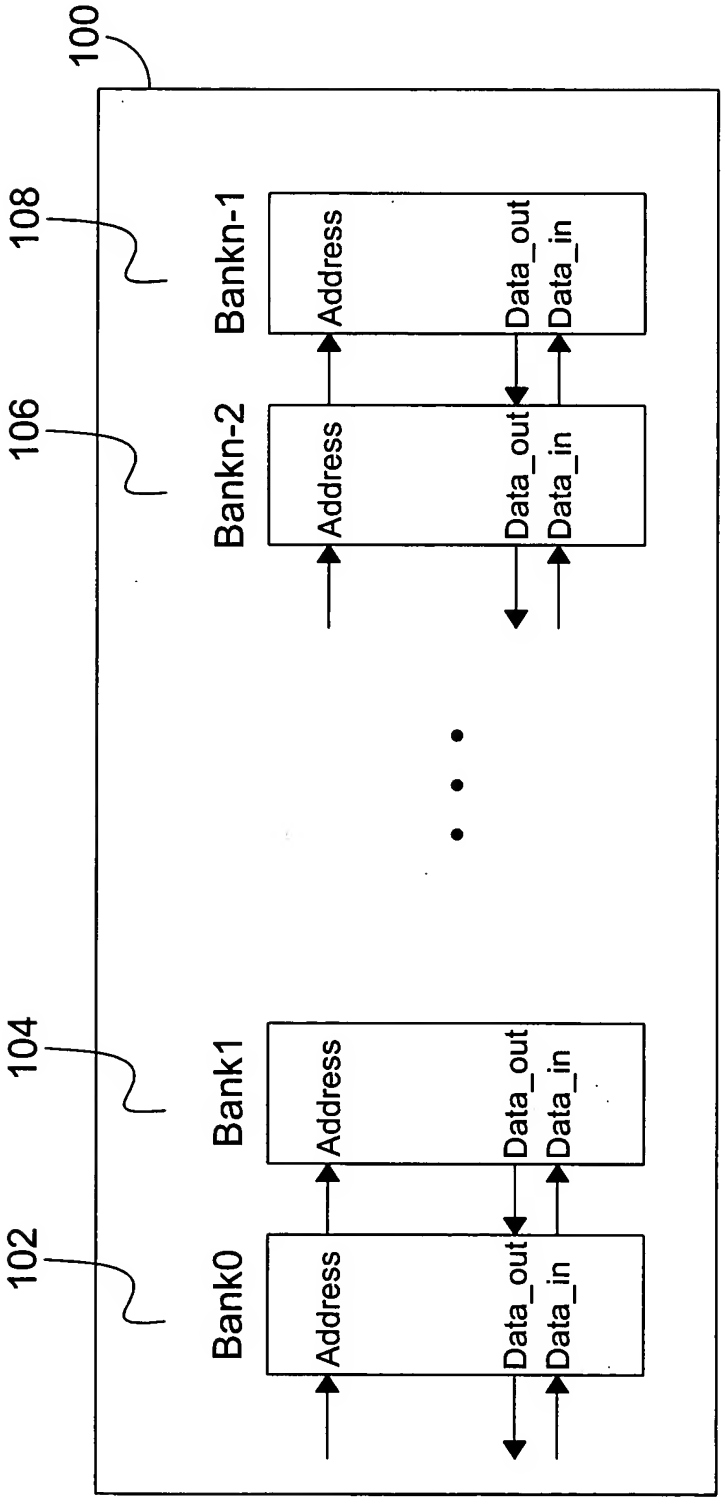

FIG. 1(a)

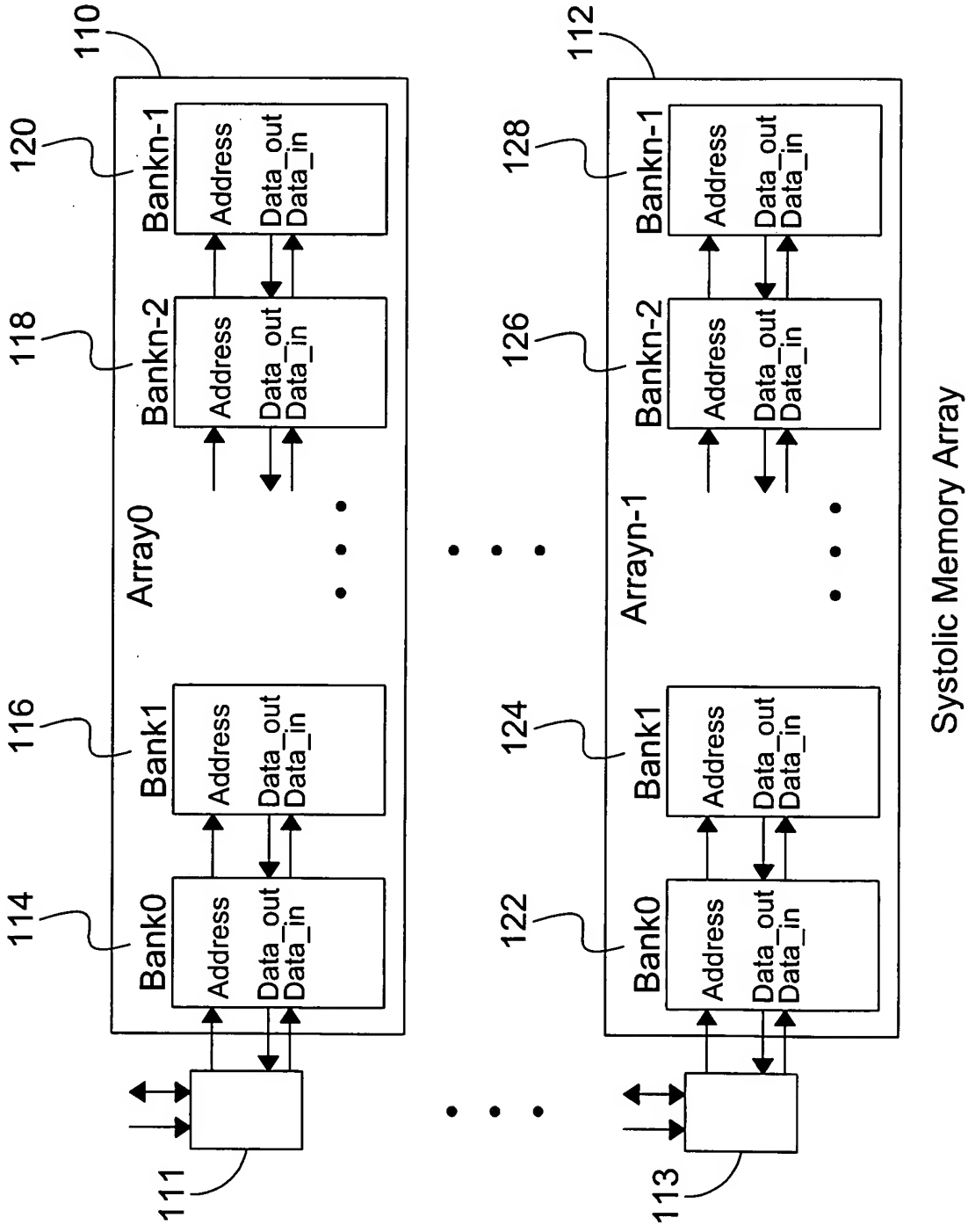
110
112
120
128
Bankn-1
Address
Data_out
Data_in
118
126
Bankn-2
Address
Data_out
Data_in
Array0
Arrayn-1
116
124
Bank1
Address
Data_out
Data_in
114
122
Bank0
Address
Data_out
Data_in
111
113
Systolic Memory Array

FIG. 1(b)

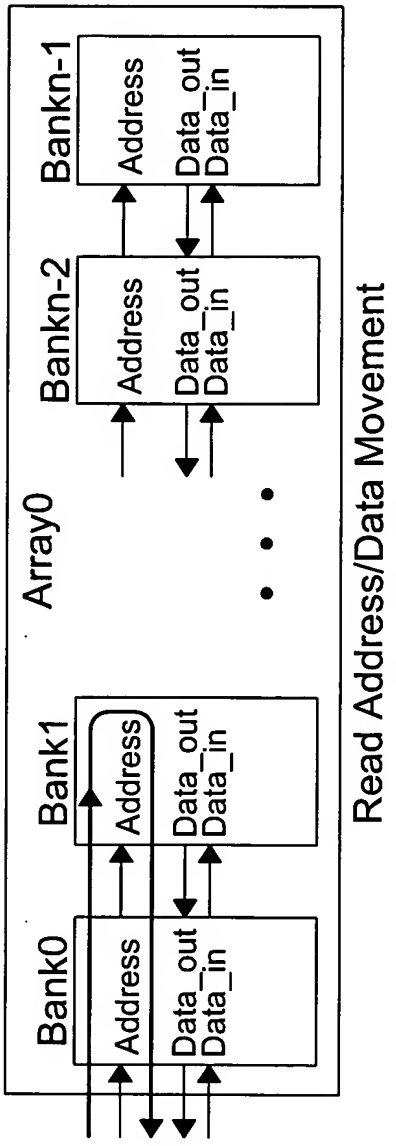
Array0
Bank0
Address
Data_out
Data_in
Bank1
Address
Data_out
Data_in
Bankn-2
Address
Data_out
Data_in
Bankn-1
Address
Data_out
Data_in
Read Address/Data Movement

FIG. 2(a)

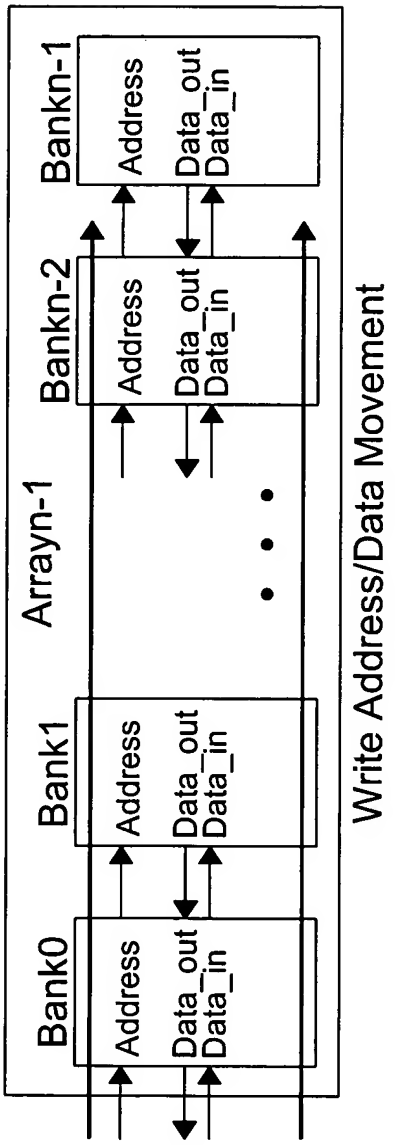
Arrayn-1
Bank0
Address
Data_out
Data_in
Bank1
Address
Data_out
Data_in
Bankn-2
Address
Data_out
Data_in
Bankn-1
Address
Data_out
Data_in
Write Address/Data Movement

FIG. 2(b)

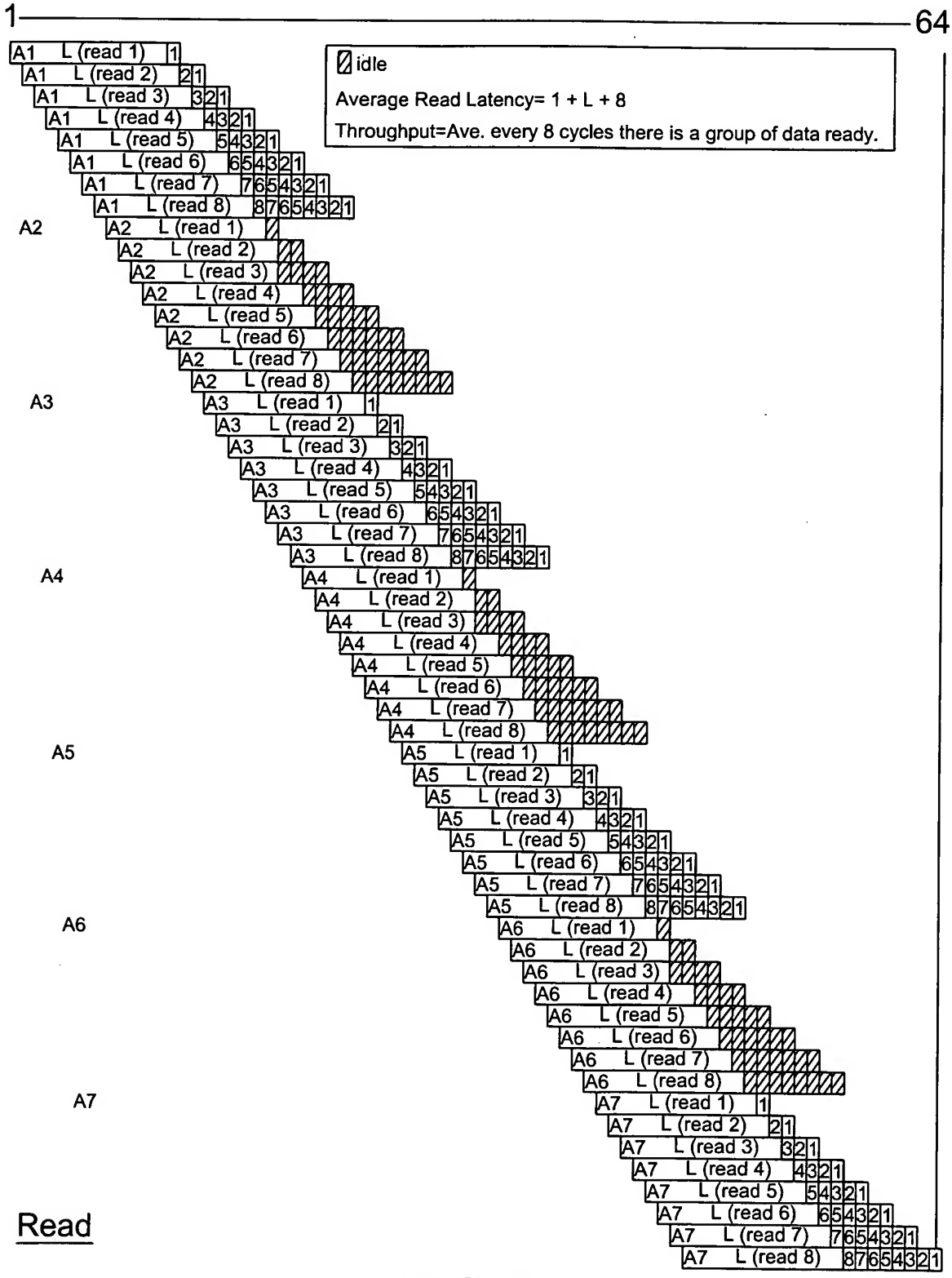
1
64
idle
Average Read Latency= 1 + L + 8
Throughput=Ave. every 8 cycles there is a group of data ready.
A1 L (read 1) 1
A1 L (read 2) 21
A1 L (read 3) 321
A1 L (read 4) 4321
A1 L (read 5) 54321
A1 L (read 6) 654321
A1 L (read 7) 7654321
A1 L (read 8) 87654321
A2
A2 L (read 1)
A2 L (read 2)
A2 L (read 3)
A2 L (read 4)
A2 L (read 5)
A2 L (read 6)
A2 L (read 7)
A2 L (read 8)
A3
A3 L (read 1) 1
A3 L (read 2) 21
A3 L (read 3) 321
A3 L (read 4) 4321
A3 L (read 5) 54321
A3 L (read 6) 654321
A3 L (read 7) 7654321
A3 L (read 8) 87654321
A4
A4 L (read 1)
A4 L (read 2)
A4 L (read 3)
A4 L (read 4)
A4 L (read 5)
A4 L (read 6)
A4 L (read 7)
A4 L (read 8)
A5
A5 L (read 1) 1
A5 L (read 2) 21
A5 L (read 3) 321
A5 L (read 4) 4321
A5 L (read 5) 54321
A5 L (read 6) 654321
A5 L (read 7) 7654321
A5 L (read 8) 87654321
A6
A6 L (read 1)
A6 L (read 2)
A6 L (read 3)
A6 L (read 4)
A6 L (read 5)
A6 L (read 6)
A6 L (read 7)
A6 L (read 8)
A7
A7 L (read 1) 1
A7 L (read 2) 21
A7 L (read 3) 321
A7 L (read 4) 4321
A7 L (read 5) 54321
A7 L (read 6) 654321
A7 L (read 7) 7654321
A7 L (read 8) 87654321
Read

FIG. 3

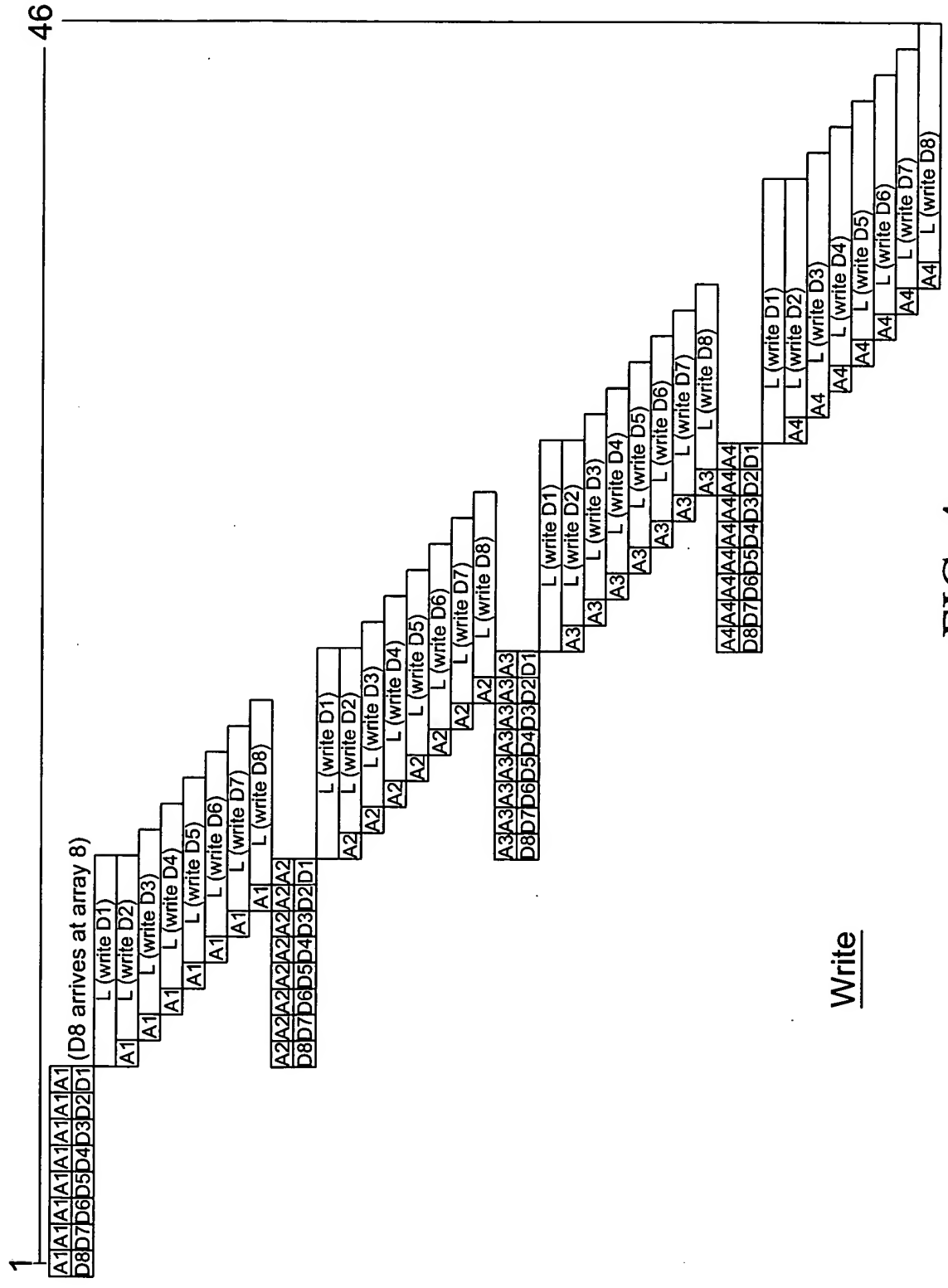
1
46
A1A1A1A1A1A1A1A1
D8D7D6D5D4D3D2D1
(D8 arrives at array 8)
L (write D1)
L (write D2)
L (write D3)
L (write D4)
L (write D5)
L (write D6)
L (write D7)
L (write D8)
A1
A2A2A2A2A2A2A2A2
D8D7D6D5D4D3D2D1
A3A3A3A3A3A3A3A3
D8D7D6D5D4D3D2D1
A4A4A4A4A4A4A4A4
D8D7D6D5D4D3D2D1
Write

FIG. 4

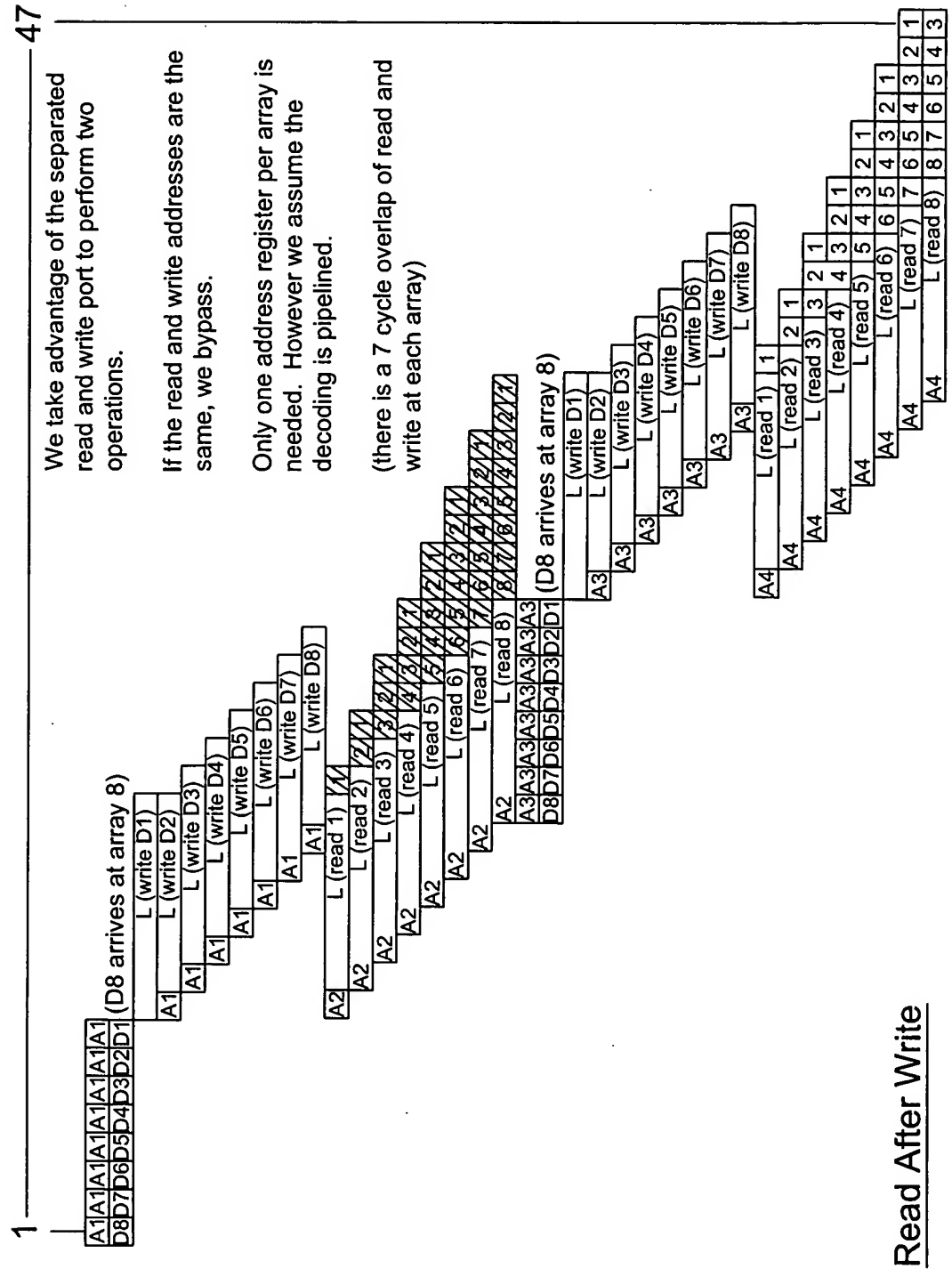
1
47
We take advantage of the separated read and write port to perform two operations.
If the read and write addresses are the same, we bypass.
Only one address register per array is needed. However we assume the decoding is pipelined.
(there is a 7 cycle overlap of read and write at each array)
(D8 arrives at array 8)
L (write D1)
L (write D2)
L (write D3)
L (write D4)
L (write D5)
L (write D6)
L (write D7)
L (write D8)
L (read 1)
L (read 2)
L (read 3)
L (read 4)
L (read 5)
L (read 6)
L (read 7)
L (read 8)
Read After Write

FIG. 5

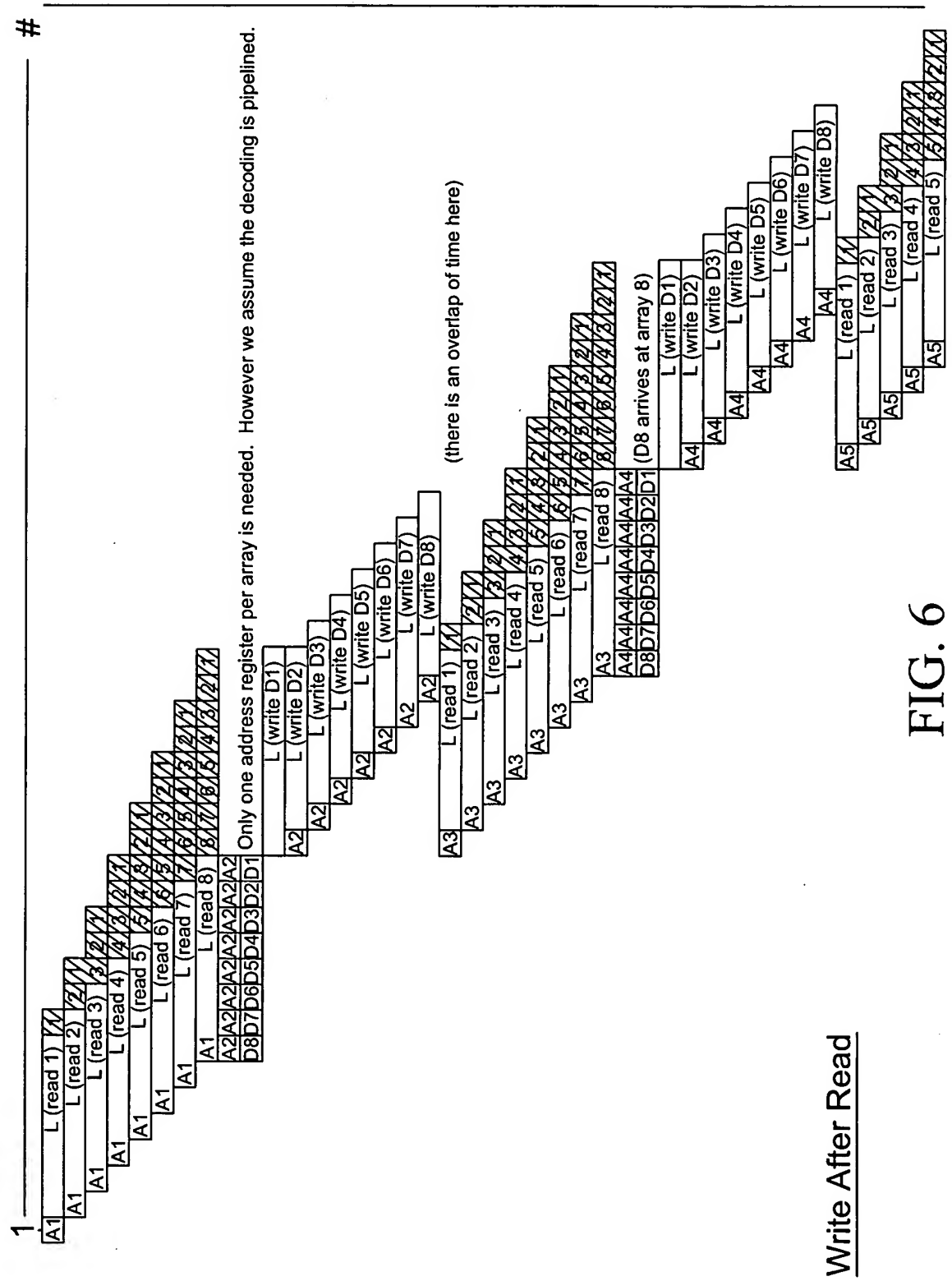

FIG. 6

Write After Read

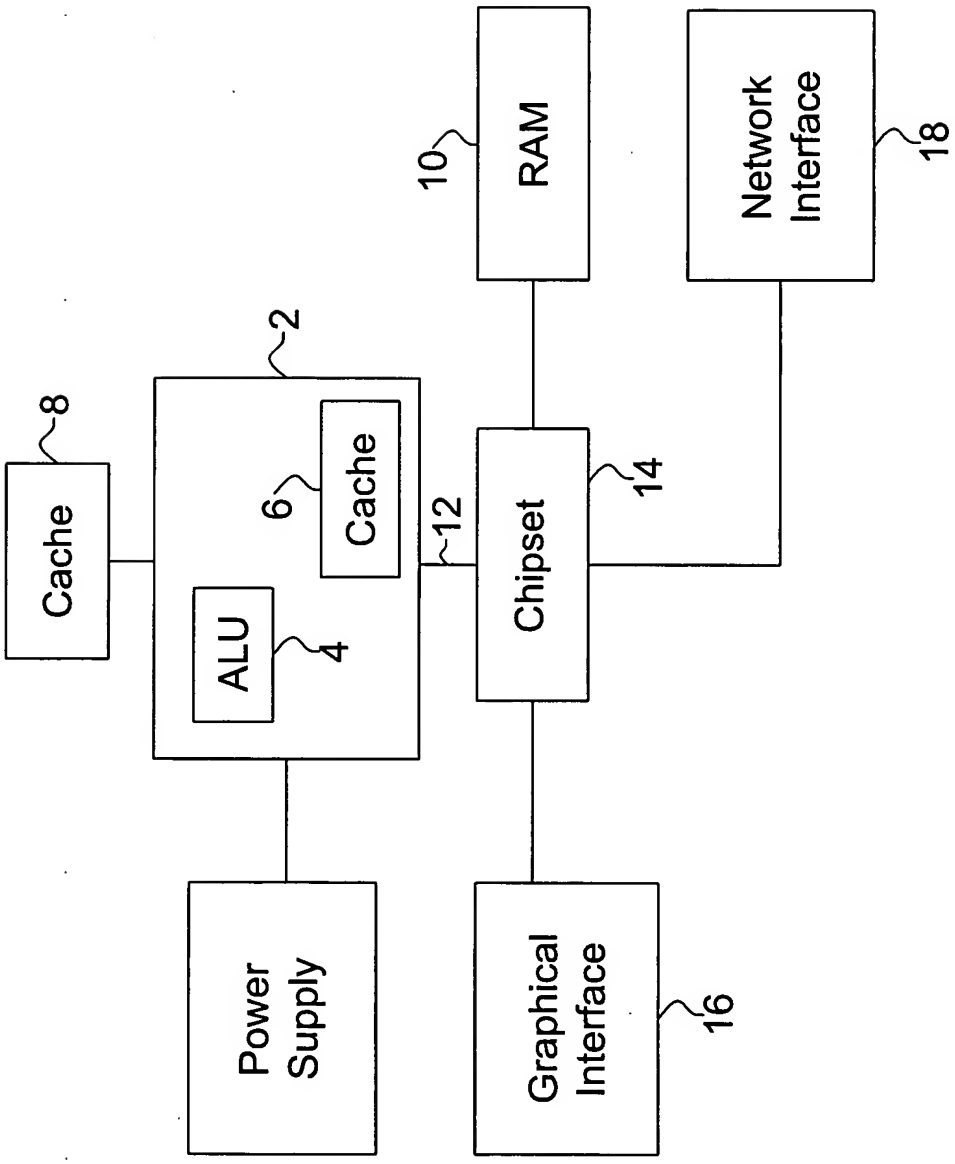
RAM
10
Network Interface
18
2
8
Cache
6
Cache
12
Chipset
14
ALU
4
Power Supply
Graphical Interface
16

FIG. 7